REMARKS

Claims 1-17, 30-38 were rejected under 35 U.S.C. 102(b) over Yaegashi et al., U.S. patent no. 6,265,739.

Claim 1 is supported by the original disclosure as follows:

> (b) forming a first layer **(140 in Figs. 13A, 13B)** ... to provide (i) the select gate **(Fig. 29A)**..., and (ii) a gate for the first peripheral transistor **(Fig. 29B)**...;
>
> (c) **after forming the first layer**, forming one or more second layers **(160 in Fig. 17 and 170 in Figs. 21A-21B)** which provide the floating gates **(FG 160 in Fig. 29A)**....

Claim 1, and the remaining claims, are not limited to the embodiments discussed herein.

The Examiner states:

> In re claim 1, **Yaegashi** discloses ... (b) forming a first layer ... and patterning the first layer to provide (i) the select gate ... **(SELECT TRANSISTOR)**, and (ii) a gate for the first peripheral transistor ... **(Vpp-Tr)** (col. 8, lines 41-54); (c) ***after forming the first layer***, forming one or more second layers which provide the floating gates **(106, in MEMORY CELL region) and the control gates (*106*, in MEMORY CELL region)** ... (FIGS. 1-4B).

This is respectfully traversed. First of all, Yaegashi's control gates are made from layer 107, not 106, as acknowledged by the Examiner on page 2 of the office action (control gates "**107,** in MEMORY CELL region"). Secondly, Yaegashi's select gate in the SELECT TRANSISTOR region and the peripheral gate in the Vpp-Tr region are made from the same layer 106 as the floating gates. Yaegashi, column 8, lines 7 and 40-41. Therefore, Yaegashi's layers (106, 107) formed to provide the floating and control gates are **not** formed ***after*** the layer (106) formed to provide the SELECT TRANSISTOR gate and the Vpp-Tr gate as asserted by the Examiner. Forming the layer 106 is part of forming the layers 106, 107, and therefore forming the layers 106, 107 is not performed ***after*** forming the layer 106.

The Examiner states on page 8 of the Office Action:

> ... It is noted that the features upon which applicant relies (i.e., forming the floating gate layer after the select or peripheral transistor gate layer) are not explicitly recited in the rejected claim(s) since Applicant's claimed invention has a layer and a layer can be at any location.

This statement is not understood. Clarification is requested.

Claim 32 further recites:

> ... ***after*** forming the first layer but ***before*** forming the one or more second layers, forming a dielectric ("floating gate dielectric") ... to separate the floating gates from the substrate.

In Yaegashi's Fig. 4A, the floating gates 106 (MEMORY CELL) are separated from substrate 101 by dielectric 105. Dielectric 105 is **not** formed ***after*** the layer 106 as recited in Claim 32.

Claim 33 further recites that the floating gate dielectric is formed ***after*** the operation (b1) of patterning the first layer to provide the select gate.

In Yaegashi, the dielectric 105 is **not** formed ***after*** the patterning of layer 106 as in Claim 33.

Any questions regarding this case can be addressed to the undersigned at the telephone number below.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 21, 2005.

Michael Shenker 3-21-05
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

Michael Shenker

Michael Shenker
Patent Attorney
Reg. No. 34,250
Telephone: (408) 392-9250, Ext. 212

Law Offices Of
MacPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110